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08EC032

M.Tech. Degree Examination, May/June 2010
Digital System Design using VHDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain entity and data flow modeling, with examples. **(06 Marks)**
b. Write a behavioral description of JK flip-flop with active low clock, set and reset using process statement. **(06 Marks)**
c. Write a structural description of 4-bit adder. **(08 Marks)**

2 a. Explain the following with examples: i) Loop statement ii) Case statement iii) Assert statement iv) Wait statement **(12 Marks)**
b. Write a VHDL model for the 74194 4-bit bidirectional shift register, with following functions. The CLR_b input is asynchronous and active low and overrides all the other control inputs. If the control inputs $S_1 = S_0 = 1$, the register is loaded in parallel. If $S_1=1$ and $S_0=0$, the register is shifted right and SDR (Serial Data Right) is shifted into Q_3. If $S_1=0$ and $S_0=1$, the register is shifted left and SDL is shifted into Q_0. If $S_1=S_0=0$, no action occurs. **(08 Marks)**

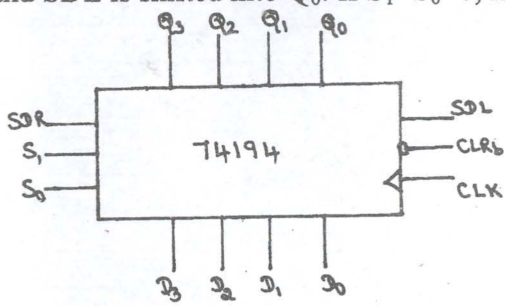

Fig. Q2 (b)

3 a. Bring out the differences between a VHDL function and a VHDL procedure. **(05 Marks)**
b. Write a VHDL function that adds two 4-bit vectors and a carry and it returns a 5 bit sum. **(05 Marks)**
c. List the data types in VHDL. Explain any three types with example, showing type declaration and object declaration of that type. **(10 Marks)**

4 a. Draw the block diagram, state graph and VHDL program for the behavioral model of a 4×4 multipler. **(12 Marks)**
b. Write a VHDL description for a divider that divides a 8-bit dividend by a 3-bit divisor to give a 5-bit quotient. **(08 Marks)**

5 a. Give an execution graph and develop a micro VHDL description of a system that performs the following computation without using a two-operand adder.
Inputs : $x, y \in \{-128,\ldots\ldots 127\}$
Output: $z \in \{-256,\ldots\ldots\ldots 508\}$

$$\text{Function : } z = \begin{cases} \dfrac{4[(x+|y|)]}{2} & \text{if } x < |y| \\ 4x & \text{otherwise} \end{cases}$$
(10 Marks)

b. Classify the control of the system according to its structure and explain. **(05 Marks)**
c. What are the characteristics of the implementation of an RTL system at the binary level? **(05 Marks)**

6 a. Outline the procedure for designing RTL systems with necessary generalized VHDL descriptions for data subsystem and control subsystem. **(10 Marks)**

b. Explain structure of a micro programmed controller, with block a diagram. **(10 Marks)**

7 a. Draw the general structure of a data sub system, suitable for RTL sequence of a micro programmed system and explain the functions of the various modules. **(10 Marks)**

b. Write the VHDL behavioral description of the above data subsystem. **(10 Marks)**

8 a. Draw the flowchart and SM chart for floating point multiplication. **(10 Marks)**

b. Draw the internal organization and timing diagram for a memory subsystem suitable for a typical microcomputer. **(05 Marks)**

c. Write a VHDL description using case statement for 2-to-4 decoder. **(05 Marks)**

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